ABSTRACT OF THE DISCLOSURE

A first transistor is arranged between a reference voltage node and a first node, and is connected at its gate to a second node. A second transistor is arranged between the second node and the reference voltage node, and is connected at its gate to the first node. Charges are supplied to the first and second nodes via capacitance elements receiving first and second control signals, respectively. Further, a third transistor is arranged between the second node and an output node, and is connected at its gate node to a third control signal ϕCT via a third capacitance element. A fourth transistor is connected between the output node and a gate node of the third transistor, and is connected at its gate to the second node. An internal voltage at an intended level can be generated with low power consumption while efficiently using charges without causing an ineffective current flow.